Silicon Innovation: Leaping from 90 nm to 65 nm

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Overview: Built-in Capabilities Enable New Services

You know what you want to be able to do; you just need a capable platform on which to do it. Real-time voice and face recognition, faster data searches, self-reconfiguring radios, keyboard-free computing, secure networks, smaller form factors, and better multimedia—Intel's leading-edge architectures and breakthrough manufacturing processes are allowing us to design new capabilities right into the hardware and firmware of everything from cell phones to servers.

You don't have to wish anymore for more capable systems to design on. Start shifting your ideas into drive and create what you used to only dream of.

Real Advances, Real Benefits

Intel has a long history of translating technology leaps into tangible benefits. Today, Intel is translating advances in processor performance, transistor size, and 65- and 45-nanometer (nm) process technology into a generational leap of new capabilities. For example, you'll see a lot of new and improved functionality built into the desktop PCs, mobile devices, and servers that are shipping in 2006:

- Impressive multimedia performance for video, audio, and data streaming (via multi-core architecture and advanced transistor designs)
- Two new layers of hardware-based security to protect against hackers, viruses, and worms, via filters for inbound and outbound network traffic; nonvolatile memory for business-critical applications and information; and automatic presence checking for management and security agents (via Intel's advanced security technologies)
- Advanced manageability for IT, including remote device discovery, accurate inventories of PC assets, and remote problem resolution—even for PCs that are powered off or whose operating system (OS) is inoperable (via Intel® Active Management Technology)
- Acceleration technology that dramatically improves the speed that network traffic moves through the system (via Intel® I/O Acceleration Technology), for faster downloads and network communication
- Hardware-based virtualization, for IT managers who want to add another, even more robust layer of security and management to devices (via Intel® Virtualization Technology)

How We Do It

Intel is second to none in the design and high-volume precision manufacturing of advanced microprocessors and other platform ingredients. We achieve this simply by questioning assumptions, researching the problems, testing the proposals, and developing the solutions you need—at the cost and with the energy-efficient performance you demand. Today, our leading-edge technologies are delivered to you in a remarkably scaled 65-nm package that gives you the capable design platforms you need for your innovations.

It's a Small, Small Business

We live in the nano-era, where the analogy of 1/100 of a human hair is no longer relevant—with Intel's new 65-nm process, we could fit tens of thousands of transistors inside a single red blood cell. At the nanoscale, you must think in terms of atomic layers, sometimes only three or five atoms thick.

For transistors, this is a critical scale that offers tremendous opportunities for increased performance in the same size footprint—remember, size-space is a quadratic relationship. Halving the size of the transistor means four times as many transistors can be packed into the same physical space. Add in the ability to pack transistors (where energy efficiency is more important than performance), and you can now put eight transistors in the same size footprint in which only one used to fit. Cache sizes can now increase; for example, Intel has doubled cache size from 2 MB to 4 MB for desktop and laptop PCs, while cache size has jumped from 4 MB to 8 MB for servers. Two processor execution cores can now fit into the space of one, giving devices higher-end performance without increasing the footprint.

The more transistors we can pack into a chip and the faster we can make them switch, the more computing we can provide, and the more economical that computing will be.

Breakthrough Technologies and Advanced Designs

As of the last quarter of 2005, Intel is the only company in the world shipping products based on 65-nm silicon technology for revenue. Already, dual-core mobile processors and 65-nm silicon servers are shipping, while products based on our new microarchitecture are expected in the second half of 2006. The full crossover for processors, from 90 nm to 65 nm, is expected in the third quarter of 2006.

With high-performance processor architecture, breakthrough transistor materials, and an amazingly scaled process technology, Intel delivers advanced designs with real benefits for developers and users.

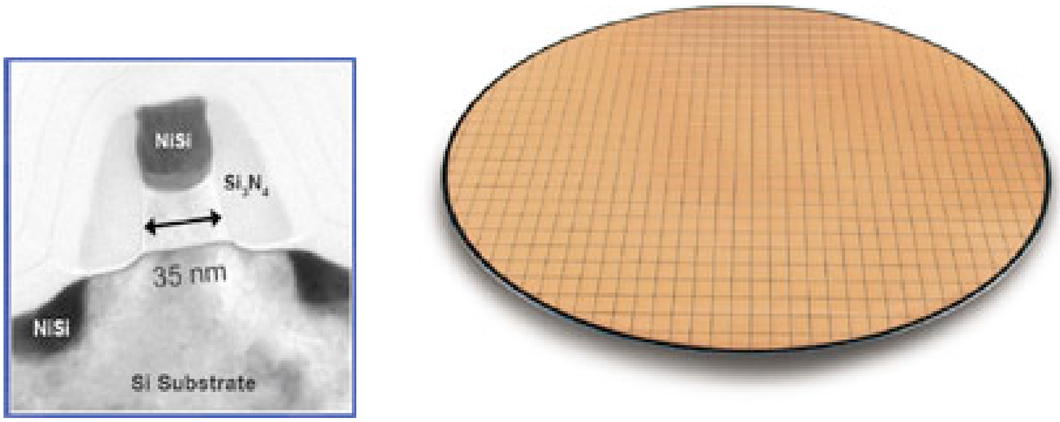

Figure 1. *Intel strained silicon (left) and a 65-nm wafer of Intel® Core™ Due processors (right).*

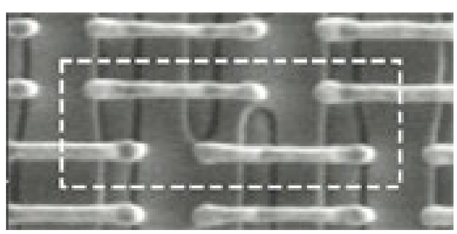

Figure 2. *These 65-nm SRAM memory cells each have six transistors packed in an area of 0.57 µm2. Some 10 million of these transistors could fit in a square millimeter—about the size of the tip of a ballpoint pen.*

Two cores for the price of one: multi-core architecture

Intel's new platforms use dual-core processors, which contain two computational or "execution" cores, and deliver (via the appropriate software) fully parallel execution of multiple software threads—an architecture that dramatically increase a processor's overall computational throughput.

However, there's much more to processor performance than just transistors. Other critical factors include processor design, amount of cache, speed of cache, and cross-interface. Because of this, Intel processors include specialized microarchitecture, such as micro-op fusion, advanced stack management, an advanced transfer-cache architecture and system bus, and advanced branch prediction architecture to improve performance even further. Future processors will include even more advanced designs.

Materials breakthroughs: High-k gate dielectric + metal gate

The primary challenge in doubling performance is power: reducing leakage (heat) while still packing more, smaller transistors (performance) into a still smaller footprint space. The transistor gate dielectrics can be taken down only to a particular thinness, because past that point, the gate insulation becomes so "porous" that too many electrons leak through.

Intel has already scaled down the traditional gate insulator (the dielectric) to as thin as 1.2 nm, the equivalent of only five atomic layers. To scale further, Intel has demonstrated a new, nonsilicon, high-capacitance (high-k) gate dielectric. Compared to silicon, the new material reduces gate leakage by a factor of more than 10,000.

The new dielectric won't work with current silicon-based gate electrodes, so Intel is combining the new high-k dielectric with a new, metal gate material—a shift that Intel expects will be one of the most significant in the evolution of the metal-oxide silicon (MOS) transistor. To make this happen, Intel must also use a new manufacturing process to lay down the new gate dielectric material one molecular level at time. The three-way combination of breakthrough dielectric, gate material, and precision fabrication process drastically reduces current leakage and delivers record transistor performance.

Energy-efficient innovations

Power efficiency is no longer just about current leakage inside a processor, but about reducing power bills in the office. Some of the advances in process technology include:

- Unique, second-generation strained silicon, which stretches or compresses the grid-like pattern that silicon atoms naturally form so electrons can flow faster with less resistance. Intel's 65-nm strained silicon technology provides significant performance advantage even at ultra-low leakage levels
- Lower capacitance inter-layer dielectrics to reduce power and increase interconnect performance

Unique, precision packaging

Intel's lead in 65-nm process for performance is matched by our advanced packaging technologies, such as new, highly conductive thermal interface materials (TIMs). Packaging houses the processor die, protects it from contamination, and acts as an interface between the silicon chip and the rest of the computer system. Intel is pioneering package designs that allow for even higher transistor density and that maximize performance by balancing electrical, thermal, and mechanical capabilities.

Extreme lithography

Intel is driving process technology to amazing levels. One example is Intel's plan to use extreme ultra-violet (EUV) lithography in the future. EUV lithography uses a series of mirrors to direct light with a wavelength of 13.5 nm to print exceptionally small features—elements as small as 32 nm and beyond.

The Amazing Microscale MEMS

Micro electro-mechanical systems, or MEMS, are mechanical structures (such as sensors and actuators) that can sense environmental changes, and actuate and move based on these changes. This is one of the interesting areas Intel is investigating to extend the application of silicon devices in the future.

MEMS require precision fabrication in order to be built directly on the silicon, and can be fairly complex, such as moveable mirrors for projection displays and optical switching, gyroscopes that monitor the motion of an automobile or building (seismic sensors), and even biochemical sensors for "wetware" applications—such as smoke or chemical detectors—for healthcare, pharmaceuticals, chemicals, and refineries. MEMS offer an increasingly wide array of opportunities for computing devices to interact with the physical world.

Intel's MEMS research has focused on developing silicon and packaging building blocks that are needed for a variety of applications in addition to addressing reliability and manufacturability. Cantilevers, wafer-scale hermetic packaging and deep silicon etching are fundamental building blocks to any MEMS application. For example, a polysilicon cantilever structure has been utilized to build an advanced 3V electrostatically actuated radio frequency (RF) switch. Such switches could be used to reconfigure radios and antennae. For example, they could adaptably control variable-length antennae for cell phones, which would allow optimal transmission and reception as the phone moves from one service area to the next, regardless of geographical boundaries and differences in frequency-use standards.

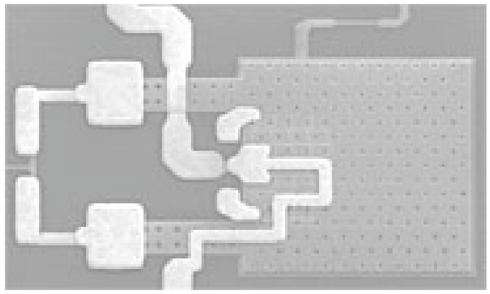

Figure 3. *Polysilicon cantilevers: An advanced 3V polysilicon switch that could be used for reconfigurable radios.*

Wafer scale packaging has been applied for combining RF switches with other circuits to build reconfigurable filters for use in multimode radios in mobile devices. Finally, deep silicon etching has been utilized to explore ultra-high-resolution (several µG) silicon + piezoelectric MEMS inertial sensors for which current state of the art is in the range of hundreds of µG (G is the acceleration due to gravity).

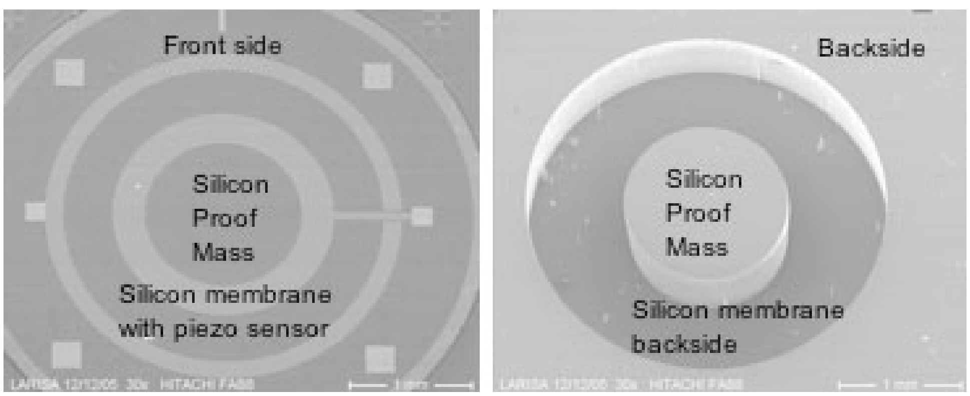

Figure 4. Deep silicon etching: Deep reative ion etching used to research ultra-high-resolution (several µG) silicon + piezoelectric inertial sensors.

Coming Next: 45-nm Chips

Intel has demonstrated fully functional SRAM chips that are a key step toward the high-volume manufacture of yet another smaller generation of technology. The 45-nm process will be Intel's next-generation process, and will provide:

* About a two-fold improvement in transistor density, for either smaller chip size or increased transistor count.
- More than a 20 percent improvement in transistor switching speed, or more than a five-fold reduction in transistor current leakage. This will make it possible to build smaller chips and extend battery life for mobile devices.

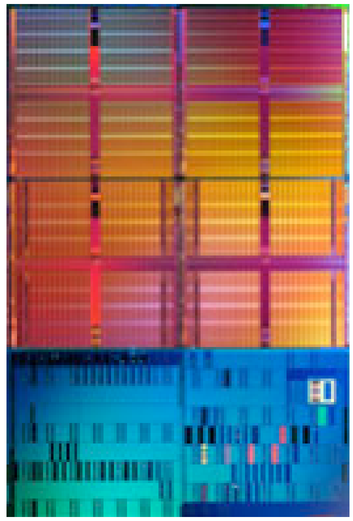

***Figure 5.** Die photo of an Intel® 45-nm shuttle test chip including 153-Mb SRAM and logic test circuits. The chip contains more than one billion transistors.*

This manufacturing process, scheduled for delivery in 2007, will offer even greater energy efficiency for mobile devices and increased opportunities for building smaller, more-powerful platforms.

Down the Road...

Intel continues to invest strongly in research that pushes technology forward, from innovative transistors to prototype materials.

Innovative structure: Tri-gate transistors

The gate is the part of a transistor whose electrical state determines whether the transistor is on or off. Intel's unique three-dimensional tri-gate transistor actually triples the space available for electrical signals to travel, without taking up more area than a planar transistor. This design not only delivers higher performance but, because of its unique structure, reduces current leakage in comparison to planar transistors. Intel has already prototyped the tri-gate transistor in gate lengths of 30 nm.

New, prototype materials

Researchers from Intel and the British company QinetiQ have jointly developed prototype transistors that show promise for future high-speed and yet very-low-power logic applications.

The prototype transistors are made of a so-called III-V compound semiconductor, indium antimonide (chemical symbol InSb). III-V materials have a higher mobility than silicon, which translates directly to a faster switching speed. Since current flows faster with less friction, these transistors don't generate as much heat as silicon.

This is an important milestone in extending the trajectory of Moore's Law well beyond 2015. The key breakthrough is the successful demonstration of an enhancement-mode InSb transistor with a gate length of only 85 nm. These transistors operate at a low supply voltage of only 0.5V, and achieve a record intrinsic speed of greater than 300 GHz. That represents a 50 percent higher speed and 6x to 10x less direct-current power dissipation as compared to state-of-the-art silicon MOSFETs.

The prototypes are the smallest enhancement-mode III-V transistors that have been made with the right threshold voltage and low parasitic leakage. Intel is now working toward possibly using these transistors in chips in the second half of the next decade.

Far-future Alternatives to Silicon

In the coming decade, Intel's process geometries will approach the physical limits of atomic structure. At atomic limits, thermal effects will eventually limit how far we can scale silicon-based transistors. At that point, it will still be possible to build electronic devices smaller than CMOS, but those devices would not operate faster or be cheaper to produce. It's unlikely that any charge-based device will be able to beat scaled CMOS.

Instead, to go beyond CMOS, the industry will have to move to alternative logic devices. Already, Intel is investigating some very interesting areas such as spintronics, quantum computing, and optical computing. These could be heterogeneously integrated onto a silicon substrate. These alternative logic devices are highly speculative, and for the immediate future, Intel continues to lead through designs that explore how far CMOS can take us, extending the trajectory of Moore's Law through advanced and breakthrough transistor and package designs.

Silicon Leadership: Framework of the Future

What does it mean to lead? It is just about being first, like Yuri Gagarin in space or Roald Amundsen to the south pole?

True leadership encompasses more than just being first. Industry leadership makes a contribution to the world, one that acts as a scaffold for new ideas and a framework for new opportunities to advance success.

Intel has consistently been that leader. Beyond delivering new processors or more performance first, Intel has created a platform of new technologies that catalyze others to develop their own creative solutions. Many of the innovations you see now in your systems, software, and peripheral hardware equipment are not actually ideas Intel realized, but products thought up and created by others who saw the opportunities and capabilities enabled by Intel's new hardware and firmware.

In a sea of technologies, someone must create the challenging platform upon which others can build something new. Intel is that structure: the company that drives the research, pushes the envelope, and makes the investments that help lead the world to the future.

More Info

You can learn much more by visiting the Silicon portion of the Intel Web site.

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R. M. Ramanathan has been a technology evangelist at Intel for the past three years, most recently in the Sales and Marketing Group. In his 11 years with Intel he has held various positions, from engineering to management. Before coming to Intel, Ramanathan was director of engineering for a multinational company in India. He has received 4 patents and has 10 patents pending in the areas of networking and security. Ramanathan holds a master's degree in mathematics from Madurai Kamaraj University in India.

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Rob Willoner is a technology analyst in Intel's Technology and Manufacturing Group. He has had a variety of positions in his 26 years at Intel, in marketing, IT, processor design, and design technology. He received his Ph.D. in computer science from the University of Alberta,
Canada, and joined Intel upon graduation.

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